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(71) Applicant *(for all designated States except US)*: **GENOA COLOR TECHNOLOGIES LTD.** [IL/IL]; P. O. Box 12209, 46733 Herzliya (IL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WEISS, Nir** [IL/IL]; Sokolov 86, 46497 Herzliya (IL). **GANOR, Avi** [IL/IL]; 11 Haodem, 73142 Shoham (IL).

(74) Agents: **EITAN, PEARL, LATZER & COHEN-ZEDEK** et al.; 7 Shenkar Street, 46725 Herzlia (IL).

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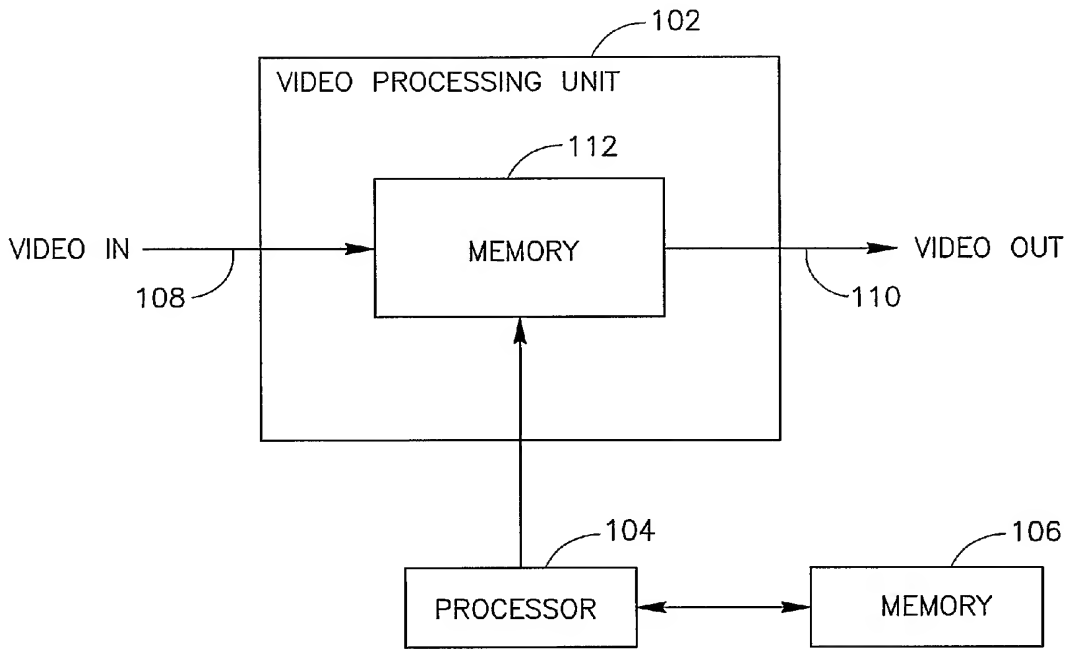
(54) **Title:** METHOD AND SYSTEM OF UPDATING A MEMORY OF A COLOR DISPLAY



(57) **Abstract:** Embodiments of the invention include a method, device and/or system for displaying a color image. The method may include, for example, correlating between a memory update time period, during which data stored in a memory is being updated, and an idle time period, during which a color image frame is not being updated based on data retrieved from the memory during the idle time period. Other embodiments are described and claimed.

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METHOD AND SYSTEM OF UPDATING A MEMORY OF A COLOR DISPLAY

Cross reference to Related Applications

This application claims the benefit of US Provisional Patent Application, 60/535,541, filed January 12, 2004, the disclosure of which is incorporated herein by reference in its entirety.

Field Of The Invention

The invention relates to updating a memory of a color display.

Background

Fig. 1 schematically illustrates a conventional video processing unit 102. Unit 102 may receive and process a video signal 108 to produce an output video signal 110. Unit 102 may implement at least one, e.g., internal, memory 112 as part of the processing of signal 108. Memory 112 may be adapted to receive an input, e.g., including signal 108, and provide an output, e.g., including signal 110, corresponding to the received input. For example, memory 112 may include a Look Up Table (LUT) as is known in the art.

A processor 104 may be implemented to update the data stored in memory 112, for example, in accordance with an adjustment made to one or more display parameters, e.g., contrast, brightness, color saturation, sharpness, color temperature and/or dynamic noise reduction. The display parameters may be controlled and/or adjusted during operation of the display device, e.g., while the device displays an image. Some of the parameters may be adjusted by a user, which may, for example, manually adjust one or more of the parameters and/or select a pre-defined mode of operation, e.g., defining a setting of one or more of the parameters. Some of the parameters may be controlled and/or adjusted automatically, e.g., without the user's knowledge and/or participation. For example, a dynamic contrast parameter, which may affect the brightness, contrast and/or gamma parameters as a function of video frame content, may be automatically adjusted as part of a process performed by the device. The number of parameters that

may be controlled and/or adjusted during operation of the device may depend on the complexity enabled by the display device.

Processor 104 may calculate updated data, e.g., corresponding to one or more adjusted display parameters, to be stored in memory 112 and/or retrieve the updated data from another, e.g., external, memory 106. Processor 104 may download the updated data to a desired space in memory 112. For example, a gamma parameter may be stored as a table representing a required power behavior as a function of an input level, as is known in the art. Adjusting the gamma parameter of the display may include updating the gamma table, e.g., by downloading adjusted parameters into a memory space of memory 112 allocated for the current active gamma table.

Downloading the updated data from processor 104 to memory 112 may interrupt the flow of the processed video data, if performed simultaneously with an attempt to retrieve data from a certain address in memory 112. This interruption may occur since the data may erroneously be retrieved from the data address being updated in memory 112. For example, if processor 104 downloads updated data, D(n), into an address, A(n), in memory space 112, a simultaneous attempt, e.g., by video processing unit 102, to retrieve other data, D(m), from another address, A(m), may erroneously result in retrieving data D(n) instead of data D(m).

It may be desired to minimize or, if possible, to eliminate any interruption to the flow of the processed video data during downloading of the updated data to memory 112. This may be especially desired in order to perform dynamic adjusting of display parameters. For example, it may be desired to perform dynamic contrast correction without interrupting the video flow and/or without reducing the quality of the displayed image.

One solution for the problem described above may include using specially designed dual-space memories, e.g., including a first space address and a second space address to store the data to be updated and the updated data, respectively. After the updated data has been downloaded to the memory, a fast switch between the two memory space addresses may be performed. Alternatively, a dual port RAM, as is known in the art, may be used. Since display devices may require a relatively large amount of memory

space, the use of such dual-space memories may be ineffective and/or relatively expensive. Furthermore, switching between the two memory space addresses may require a relatively long time period if a relatively large memory is used.

Other solutions may include using an image buffer to "freeze" the image, downloading the updated data, and "de-freezing" the image. However, a system implementing such a solution may be relatively expensive. Furthermore, interruptions in the displayed image may be apparent to the user, e.g., in cases where automatic updates of the display parameters are performed frequently, often resulting in erratic and irregular video flow.

Summary of Embodiments of the Invention

Some exemplary embodiments of the invention include devices, systems and/or methods for correlating between a memory update time period, during which data stored in a memory is being updated, and an idle time period, during which a color image frame is not being updated based on data retrieved from the memory during the idle time period. Correlating between the idle time period and the memory update time period may include, for example, controlling at least one of the idle time period and the memory update time period, such that the memory update time period at least partially overlaps the idle time period.

A color display device for displaying a color image frame may include, according to some exemplary embodiments of the invention, a controller to control at least one of the memory update time period and an idle time period.

According to some exemplary embodiments of the invention the idle time period may include a time period during which no data is being retrieved from the memory. For example, the memory may be updated during a time period wherein no video data is displayed, e.g., a time period between the end of the scanning of one line, row, and/or frame of image data, and the beginning of the scanning of a consecutive line, row, and/or frame of image data. The color display device may also include, according to these exemplary embodiments, a buffer to receive updated data for updating the memory, wherein the controller is able to control the buffer to selectively update the memory with the updated data during the memory update time period.

According to other exemplary embodiments of the invention, data previously retrieved from the memory may be used for updating a displayed frame during the memory update time period. According to these exemplary embodiments, the idle time period may include a time period during which a pixel of the displayed frame is being updated based on data corresponding to a previously updated pixel. The color display device may include, for example, a selector for selecting between data retrieved from the memory corresponding to the pixel to be updated, and the data corresponding to the previously updated pixel.

According to some exemplary embodiments of the invention, the device may also include a demultiplexer to receive a multiplexed input signal including the updated data and image data corresponding to the frame, and to separate between the updated data and the image data, based on at least one timing signal corresponding to the frame.

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Brief Description Of The Drawings

The invention will be understood and appreciated more fully from the following detailed description of embodiments of the invention, taken in conjunction with the accompanying drawings of which:

Fig. 1 is a schematic block diagram of a conventional video processing system;

Fig. 2 is a schematic block diagram of an image data processing arrangement in accordance with one exemplary embodiment of the invention;

Fig. 3 is a schematic block diagram of an image data processing arrangement in accordance with another exemplary embodiment of the invention;

Fig. 4 is a schematic block diagram of an image data processing arrangement in accordance with yet another exemplary embodiment of the invention;

Fig. 5 is a schematic illustration of a flow chart of a method for processing image data in accordance with exemplary embodiments of the invention;

Fig. 6 is a schematic block diagram of a spatial processing arrangement in accordance with exemplary embodiments of the invention; and

Fig. 7 is a schematic block diagram of an image data processing arrangement in accordance with yet another exemplary embodiment of the invention.

It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn accurately or to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity or several physical components included in one element. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements. It will be appreciated that these figures present examples of embodiments of the present invention and are not intended to limit the scope of the invention.

Detailed Description Of Embodiments Of The Invention

In the following description, various aspects of the present invention will be described. For purposes of explanation, specific configurations and details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details presented herein. Furthermore, some features of the invention relying on principles and implementations known in the art may be omitted or simplified to avoid obscuring the present invention.

Some portions of the following detailed description are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art. An algorithm is here, and generally, considered to be a self-consistent sequence of acts or operations leading to a desired result. These include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like. It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices. In addition,

the term "plurality" may be used throughout the specification to describe two or more components, devices, elements, parameters and the like.

Embodiments of the present invention may include apparatuses for performing the operations herein. These apparatuses may be specially constructed for the desired purposes, or they may comprise a general-purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), electrically programmable read-only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs), magnetic or optical cards, a Dynamic RAM (DRAM), a Synchronous DRAM (SD-RAM), a Flash memory, a volatile memory, a non-volatile memory, a cache memory, a buffer, a short term memory unit, a long term memory unit, or any other type of media suitable for storing electronic instructions, and capable of being coupled to a computer system bus.

The processes and displays presented herein are not inherently related to any particular computer or other apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the desired method. The desired structure for a variety of these systems will appear from the description below. In addition, embodiments of the present invention are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the invention as described herein.

Some exemplary embodiments of the invention include devices, systems and/or methods for correlating between a memory update time period, during which data stored in a memory is being updated, and an idle time period, during which a color image frame is not being updated based on data retrieved from the memory during the idle time period. Correlating between the idle time period and the memory update time period may include, for example, controlling at least one of the idle time period and the memory

update time period, such that the memory update time period at least partially overlaps the idle time period, as described in detail below.

According to some exemplary embodiments of the invention the idle time period may include a time period during which no data is being retrieved from the memory. For example, the memory may be updated during a time period wherein no video data is displayed, e.g., a time period between the end of the scanning of one line, row, and/or frame of image data, and the beginning of the scanning of a consecutive line, row, and/or frame of image data, as described below.

Reference is made to Fig. 2, which schematically illustrates an image data processing arrangement 200 in accordance with one exemplary embodiment of the invention.

According to exemplary embodiments of the invention, arrangement 200 may include a processing unit 201, e.g., a video processing unit. For example, unit 201 may include a video interface 204 to receive an image data input signal 202, e.g., a video input signal as is known in the art, and to provide an image data output, e.g., including a video data signal 206, and at least one video control signal 208. Unit 201 may also include at least one, e.g., internal, memory 222, from which a processed video signal 220 may be retrieved, e.g., corresponding to signal 206 and to data stored in memory 222. Memory 222 may include any suitable type of memory, for example, a single port RAM, as is known in the art. A processor 214 may be associated with memory 222. Processor 214 may be capable of updating memory 222 with updated data, for example, corresponding to one or more display parameters, e.g., as are known in the art. Processor 214 may include any suitable type of processor known in the art, for example, an ARM TDMI processor, e.g., an ML674001 processor manufactured by Oki Semiconductor, a division of Oki America, Inc., a subsidiary of Oki Electric Industry Co., Ltd. Tokyo, Japan, an 8051 processor, e.g., an AN2131QC processor manufactured by Cypress Semiconductor Corp CA, or any other suitable processor. Processor 214 may calculate the updated data and/or receive the updated data from an, e.g., external, memory 216, as is known in the art.

According to exemplary embodiments of the invention, arrangement 200 may further include a controller 210 to control downloading of the updated data from processor 214 to memory 222, as described below. According to some exemplary embodiments of the invention, controller 210 may be incorporated as part of unit 201. According to other embodiments, controller 210 may be external to unit 201. For example, controller 210 may be incorporated as part of processor 214, e.g., as described below.

In some embodiments, the video data format provided to the display may include time periods during which video data of signal 206 is not displayed. According to some exemplary embodiments, the video data may have a format corresponding to a video data format used by a Cathode Ray Tube (CRT) display, as described below. However, according to other embodiments of the invention, the video data format may include any other desired video format that includes one or more time periods during which video data of data signal 206 is not displayed. Such time periods may include time periods during which data from memory 222 is not being retrieved.

In some exemplary embodiments, the video data format provided to the display may be based, for example, on the operation of a Cathode Ray Tube (CRT), which implements an electron beam for displaying an image using a scanning method, as is known in the art. In CRT display systems, as are known in the art, the electron beam is retracted after scanning each line and/or frame of the display, and no data is displayed during the time periods corresponding to retracting the electron beam. It will be appreciated by persons skilled in the art that the time period during which the electron beam is retracted after each frame may be longer than the time period during which the electron beam is retracted after each line. Accordingly, video data signal 206 may include "blank" periods corresponding to the time periods ("no data" time periods) during which the electron beam is retracted, e.g., the time periods between the end of the scanning of one line, row, and/or frame of data and the beginning of the scanning of a successive line, row and/or frame of data.

Video control signal 208 may include at least one of a vertical synchronization ("Vsync") signal, a horizontal synchronization ("Hsync") signal and a data enable ("DE")

signal. The Hsync timing signal may relate to the time period between the scanning of two consecutive lines and the Vsync timing signal may relate to the time period between scanning two consecutive frames. The DE timing signal may be a binary signal corresponding to the "no data" time periods of signal 206 and the time periods during which signal 206 provides video data to be displayed, respectively. For example, the DE signal may have a value zero during time periods corresponding to the Hsync and Vsync time periods and a value one in other time periods.

According to exemplary embodiments of the invention, controller 210 may correlate between memory update time periods, during which processor updates memory 222, and idle time periods, e.g., relating to the "no data" time periods. For example, controller 210 may be able to control the memory update time periods such that the memory time periods at least partially overlap the idle time periods. Controller 210 may be adapted, for example, to control processor 214 to download the updated data to memory 222, for example, only during idle time periods related to the "no data", e.g., the Hsync and/or Vsync, time periods. It will be noted that downloading the updated data from processor 214 to memory 222 during the "no data" time periods may have no effect on the displayed image since no data is being retrieved from memory 222 during these time periods, as described above.

According to exemplary embodiments of the invention, controller 210 may receive from interface 204 at least one signal 208, e.g., including the Hsync, Vsync and/or DE signals. Controller 210 may include any suitable hardware and/or software adapted to provide processor 214 with a "ready" signal 212, e.g., only during "no data" time periods. Processor 214 may be adapted to download the updated data to memory 222, for example, only upon receiving signal 212 from controller 210. According to some exemplary embodiments of the invention, controller 210 may control processor 214 using the Vsync signals such that the updated data is downloaded to memory 222 during the time periods between two consecutive frames. Controller 210 may additionally or alternatively control processor 214 using the Hsync signals such that the updated data is downloaded to memory 222 during the time periods between consecutive lines. Alternatively, controller 210 may control processor 214 using the DE signals such that

the updated data is downloaded to memory 222 during the time periods between consecutive frames and the time periods between consecutive lines.

According to some embodiments of the invention, arrangement 200 may not include controller 210. Instead, in such embodiments, processor 214 may be adapted to directly receive from interface 204 the Hsync, Vsync and/or DE signals and, based on the received signals, to download the updated data to memory 222 during a time period at least partially overlapping the idle time periods, e.g., during time periods including at least some of the "no data" time periods.

The rate at which the updated data is downloaded from processor 214 to memory 222 may be related to a CPU clock of processor 214.

Another exemplary embodiment of the invention provides a processing arrangement capable of updating the memory at a rate different from, e.g., higher than, the processing rate of the CPU clock of the processor, as described below.

Reference is made to Fig. 3, which schematically illustrates an image data processing arrangement 300 according to another exemplary embodiment of the invention.

According to exemplary embodiments of the invention, arrangement 300 may include a processing unit 301 including a video interface 304 and a memory 322 to receive from interface 304 a video data signal 306, e.g., similar to interface 204, memory 222 and signal 206, respectively, described above with reference to Fig. 2. A processor 314 may calculate and/or receive from an, e.g., external, memory 316 updated data to be downloaded to memory 322, e.g., as is known in the art.

Arrangement 300 may also include a buffer 326 to receive the updated data from processor 314 and to download the updated data to memory 322, as described below. Processor 314 may download the updated data to buffer 326 at a rate corresponding to the CPU clock of processor 314, while buffer 326 may download the updated data to memory 322 at a different, e.g., higher, processing rate corresponding to another clock, e.g., an internal clock of processing unit 301.

Arrangement 300 may also include a controller 310 to control the operation of buffer 326, as described below. Controller 310 may receive at least one control signal

308, e.g., including an Hsync timing signal, a Vsync timing signal and/or a DE timing signal, from interface 304, e.g., as described above with reference to Fig. 2. Based on signal 308, controller 310 may provide a "ready" signal 328 to buffer 326, e.g., during an idle time period, e.g., relating to time periods corresponding to the Vsync, Hsync, and/or DE timing signals, e.g., as described above. Buffer 326 may be adapted to download the updated data to memory 322 upon receiving "ready" signal 328 from controller 310.

Controller 310 may also control operation of processor 314, e.g., via a "ready" signal 312. Controller 310 may control the amount of updated data downloaded from processor 314 to buffer 326, for example, in order to ensure that processor 314 stops downloading data to buffer 326 when buffer 326 is full. This may be achieved, for example, by not providing processor 314 with "ready" signal 312 when buffer 326 is full. The remaining updated data, i.e., the updated data not downloaded from processor 314 to buffer 326, may be downloaded, for example, during a successive idle time period during which processor 314 may be provided with a "ready" signal from controller 310.

According to some exemplary embodiments of the invention, controller 310 and/or buffer 326 may be incorporated as part of unit 301. According to other embodiments, controller 310 and/or buffer 326 may be external to unit 301. For example, controller 310 may be implemented as part of processor 314.

According to these embodiments, arrangement 300 may allow downloading the updated data from processor 314 to buffer 326 during any desired time period, for example, non-idle time periods, e.g., including time periods during which memory 322 processes video data. The updated data may be downloaded from buffer 326 to memory 322, for example, during an idle time period in a download rate relatively higher than the CPU clock of processor 314, e.g., corresponding to the internal clock of unit 301. Thus, the rate at which the updated data is downloaded to memory 322 may be relatively high, although processor 314 may have a CPU clock of a relatively slow processing rate, e.g., a processing rate of 20-50MHz.

According to exemplary embodiments of the invention, buffer 326 may have a size related to the rate at which the updated data is downloaded from buffer 326 to

memory 322, the rate at which the updated data is downloaded from processor 314 to buffer 326, and/or the duration of the idle time periods.

According to other exemplary embodiments of the invention, data previously retrieved from the memory may be used for updating a displayed frame during the memory update time period, as described below. According to these exemplary embodiments, the idle time period may include a time period during which a pixel of the displayed frame is being updated based on data corresponding to a previously updated pixel.

Reference is now made to Fig. 4, which schematically illustrates an image data processing arrangement 400 according to yet another exemplary embodiment of the invention.

According to exemplary embodiments of the invention, arrangement 400 may include a video interface 404 and a memory 422 to receive from interface 404 a video data signal 406, e.g., similar to interface 204, memory 222 and signal 206, respectively, described above with reference to Fig. 2. A processor 414 may calculate and/or receive from an, e.g., external, memory 416 updated data to be downloaded to memory 422, e.g., as is known in the art.

Arrangement 400 may also include a selector, e.g., a multiplexer 434, to receive a first signal 440 including data retrieved from memory 422, and a second signal 438 from a Flip-Flop (FF) device 436. Multiplexer 434 may provide an output signal 420 including signal 440 or signal 438 in accordance with a control signal 432 provided by processor 414, as described below.

According to exemplary embodiments of the invention, device 436 may be adapted to receive signal 420, and to provide signal 438 after a predetermined time delay, e.g., corresponding to the time period between displaying consecutive pixels. Thus, multiplexer 440 may receive processed image data, denoted D(m), corresponding to a pixel to be displayed, e.g., as received by signal 440, as well as processed image data, denoted D(m-1), of a previously displayed pixel, e.g., as received by signal 438.

According to exemplary embodiments of the invention, processor 414 may be adapted to control multiplexer 434, e.g., using control signal 432, to provide signal 420

corresponding to data D(m), e.g., as received by signal 440, when the updated data is not downloaded to memory 422. During memory update time periods, while processor 414 downloads updated data to memory 422, processor 414 may control multiplexer 434, e.g., using signal 432, to provide signal 420 corresponding to data D(m-1), e.g., as received by signal 438.

It will be appreciated by those skilled in the art that, generally, the difference between data of consecutive pixels may not be significant, e.g., $D(m) \approx D(m-1)$. Thus, in most viewing situations, users of devices according to embodiments of the invention will not detect a visible interruption to the displayed image when displaying the data of a previously displayed pixel, e.g., while updating memory 422.

According to some exemplary embodiments of the invention, the controller for controlling the idle time period and/or the memory time period may be incorporated as part of processor 414, e.g., as described above. However, it will be appreciated that according to other embodiments of the invention, the controller may be implemented, for example, by a separate unit.

According to some exemplary embodiments of the invention, processor 414 may implement a suitable algorithm for downloading the updated data to memory 422 according to a predetermined sequence in order to allow FF 436 to receive data corresponding a recently processed pixel data. For example, processor 414 may implement a download sequence whereby downloading of the updated data is performed intermittently, e.g., periodically, for example, with every second or third displayed pixel.

It will also be appreciated by those skilled in the art that arrangement 400 may be implemented at relatively low cost. For example, multiplexer 434 and FF device 436 may be readily associated with an output of a conventional video processing system, e.g., including interface 404, memory 422 and processor 414. Furthermore, it will be appreciated that arrangement 400 may be efficiently implemented even by video processing systems designed to accommodate relatively large information downloads.

According to some embodiments of the invention, one or more of interface 404, memory 422, multiplexer 434, and FF 436 may be implemented as part of a video processing unit, as is known in the art.

A method according to exemplary embodiments of the invention may include producing a multiplexed video signal including the updated data, e.g., during "no data" time periods, and the video data and, e.g., during other time periods, as described below.

Reference is now made to Fig. 5, which schematically illustrates a flow chart of a method of processing image data, e.g., including video data, according to exemplary embodiments of the invention.

According to exemplary embodiments of the invention, the method may include receiving the video data, the updated data and/or at least one video control signal, e.g., a DE control signal, as indicated at block 502.

As indicated at block 504, the method may include multiplexing the video data and the updated data to produce a multiplexed video signal, e.g., based on the control signal, such that the multiplexed video signal includes the updated data, e.g., during "no data" time periods, and the video data, e.g., during other time periods. The multiplexed signal may also include the video control signal, e.g., during at least some of the "no data" time periods and/or at least some of the other time periods.

According to exemplary embodiments of the invention, the multiplexed video signal may be produced using any suitable hardware and/or software. For example, the multiplexed video signal may be produced by a spatial processing module, e.g., as described below with reference to Fig. 6.

As indicated at block 506, the multiplexed video signal may be transferred, e.g., using a suitable link as is known in the art, to a desired module in the display device. For example, the multiplexed video signal may be transferred, e.g., via a suitable cable, to a video processing system, e.g., as described below with reference to Fig. 7.

As indicated at block 508, the method may include demultiplexing the multiplexed video signal, for example, to provide a video data signal and/or an updated data signal, e.g., as described below.

As indicated at block 509, the method may also include controllably providing at least some of the demultiplexed data, e.g., the updated data, for updating a memory, e.g., as described below.

It will be appreciated by those skilled in the art that the complexity and/or cost of display devices and/or systems implementing the method according to embodiments of the invention, may be reduced in comparison to display systems that use two or more different signals to transfer the video data, the updated data, and/or the video control signal.

Reference is made to Fig. 6, which schematically illustrates a spatial processing module 600 according to exemplary embodiments of the invention.

According to exemplary embodiments of the invention, module 600 may include a multiplexer 610 to receive a video signal 606, e.g., including video data signals. Multiplexer 610 may also receive a signal 608 including updated data, e.g., from a processor 607. Multiplexer 610 may combine signals 606 and 608 into a multiplexed video signal 612, for example, based on at least one video control signal, e.g., a DE signal 614. According to exemplary embodiments of the invention, multiplexer 610 may combine signals 606 and 608, such that signal 612 includes the updated data of signal 608, e.g., during "no data" time periods, and the video data signals, e.g., during other time periods. Signal 612 may also include the data of video control signal 614.

Module 600 may also include a frame buffer 602, for example, to provide signal 606 based on an input video data signal 604 as is known in the art. Frame buffer 602 and/or multiplexer 610 may be implemented by any suitable hardware and/or software. For example, multiplexer 610 may be implemented as part of frame buffer 602, e.g., using suitable software and/or hardware. Alternatively, frame buffer 602 and multiplexer 610 may be implemented separately.

Reference is now made to Fig. 7, which schematically illustrates an image data processing arrangement 700 according to yet another exemplary embodiment of the invention.

Although the invention is not limited in this respect, arrangement 700 may be used for receiving a multiplexed signal, e.g., signal 612 (Fig. 6), and displaying a color image frame based on the image data of the multiplexed signal, and/or updating a memory based on the memory date of the multiplexed signal.

According this embodiment, arrangement 700 may include a video interface 704 to receive a multiplexed video signal 702, e.g., including multiplexed signal 612 as described above with reference to Fig. 6, and to provide a multiplexed data signal 706 and at least one control signal, e.g., a DE control signal 708, as described above. Signal 706 may include updated data, e.g., during "no data" time periods, and video data, e.g., during other time periods, e.g., as described above with reference to Fig. 6.

According to exemplary embodiments of the invention, arrangement 700 may also include a demultiplexer 710 to receive signal 706 and/or signal 708 and to provide, e.g., based on signal 708, a signal 712 including the video data and a signal 714 including the updated data. Arrangement 700 may also include a buffer 716 to receive signal 714 and to controllably provide a signal 718 to a data-in port 723 of a memory 722, as described below. Signal 712 may be provided, for example, to an address bus 721 of memory 722, e.g., as is known in the art.

According to exemplary embodiments of the invention, arrangement 700 may also include a controller 726 to control the operation of buffer 716 and/or memory 722, such that the memory update time period during which data of memory 722 is being updated, at least partially overlaps a time period, during which data is not being retrieved from memory 722, as described below.

According to exemplary embodiments of the invention, controller 726 may receive signal 708 and control buffer 716, e.g., using a "ready" signal 720, to provide signal 718 including the updated data, for example, during the "no data" time periods. Additionally or alternatively controller 726 may control the operation of memory 722, e.g., using a "read/write" control signal 724. For example, memory 722 may store the updated data provided by signal 718, e.g., if signal 724 includes a "write" signal. Alternatively, an output video signal 728 may be retrieved from memory 722, for example, based on signal 712, e.g., if signal 724 includes a "read" signal.

Methods, devices and/or systems for converting three-dimensional color data into multi-primary color signals may implement relatively large internal memory, e.g., in order to allow efficient data conversion, for example, as described in International Application PCT/IL02/00410, filed May 23, 2002, entitled "DEVICE, SYSTEM AND

METHOD OF DATA CONVERSION FOR WIDE GAMUT DISPLAYS" and published December 12, 2002 as PCT Publication WO02/099557, the disclosure of which is incorporated herein by reference. Thus, a video processing system, e.g., as described above, may be implemented, for example, by such multi primary color systems in order to provide relatively efficient and/or non-expensive updating of the internal memory without incurring undesired interruptions to the displayed image.

Embodiments of the present invention may be implemented by software, by hardware, or by any combination of software and/or hardware as may be suitable for specific applications or in accordance with specific design requirements. Embodiments of the present invention may include units and sub-units, which may be separate of each other or combined together, in whole or in part, and may be implemented using specific, multi-purpose or general processors, or devices as are known in the art. Some embodiments of the present invention may include buffers, registers, storage units and/or memory units, for temporary or long-term storage of data and/or in order to facilitate the operation of a specific embodiment.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

CLAIMS

1. A color display device for displaying a color image, the device comprising a controller to control at least one of a memory update time period, during which data stored in a memory is being updated, and an idle time period, during which a color image frame is not being updated based on data retrieved from said memory during said idle time period, wherein said memory update time period at least partially overlaps said idle time period.

2. The device of claim 1, wherein said idle time period comprises a time period during which data is not being retrieved from said memory.

3. The device of claim 2, wherein said idle time period relates to at least one time period selected from the group consisting of, a time period between updating two consecutive lines of said frame, a time period between updating two consecutive rows of said frame, and a time period between two consecutive color image frames.

4. The device of any one of claims 1-3 comprising a buffer to receive updated data for updating said memory, wherein said controller is able to control said buffer to selectively update said memory with said updated data during said memory update time period.

5. The device of claim 4 comprising:

a demultiplexer to receive a multiplexed input signal including said updated data and image data corresponding to said frame, and to separate between said updated data and said image data, based on at least one timing signal corresponding to said frame.

6. The device of claim 5, wherein said demultiplexer is able to selectively provide said updated data to said buffer based on said at least one timing signal.

7. The device of claim 1, wherein said idle time period comprises a time period during which a pixel of said displayed frame is being updated based on data corresponding to a previously updated pixel.

8. The device of claim 7 comprising a selector for selecting between data retrieved from said memory corresponding to the pixel to be updated, and the data corresponding to said previously updated pixel.

9. The device of claim 8, wherein said controller is able to control said selector to select the data corresponding to said previously updated pixel during said memory update time period.

10. The device of claim 8 or 9, comprising a flip-flop memory to provide said selector with a previous output of said selector after a predetermined delay time period.

11. The device of any one of the preceding claims, wherein said controller is able to control at least one of said idle time period and said memory update time period based on at least one timing signal corresponding to said frame.

12. The device of claim 11, wherein said at least one timing signal comprises at least one timing signal selected from the group consisting of a horizontal synchronization timing signal, a vertical synchronization timing signal, and a data enable timing signal.

13. The device of any one of the preceding claims, wherein said memory comprises a random access memory.

14. The device of any one of the preceding claims, wherein said memory comprises a look up table.

15. The device of any one of the preceding claims, wherein said memory comprises a single port memory.

16. The device of any one of the preceding claims, wherein said color image frame comprises a more-than-three primary color image frame.

17. The device of any one of the preceding claims, wherein the data stored in said memory comprises display parameter data.

18. A method for displaying a color image, the method comprising correlating between a memory update time period, during which data stored in a memory is being updated, and an idle time period, during which a color image frame is not being updated based on data retrieved from said memory during said idle time period.

19. The method of claim 18, wherein correlating between said idle time period and said memory update time period comprises controlling at least one of said idle time period and said memory update time period, such that said memory update time period at least partially overlaps said idle time period.

20. The method of claim 18 or 19, wherein said idle time period comprises a time period during which data is not being retrieved from said memory.

21. The method of claim 20, wherein said idle time period relates to a time period selected from the group consisting of a time period between two consecutive color image frames, a time period between updating two consecutive lines of said frame, and a time period between updating two consecutive rows of said frame.

22. The method of any one of claims 18-21 comprising:

storing updated data for updating said memory; and

updating said memory with the stored data during said memory update time period.

23. The method of claim 22 comprising:

receiving a multiplexed input signal including said updated data and image data corresponding to said frame;

separating between said updated data and said image data, based on at least one timing signal corresponding to said frame.

24. The method of claim 18 or 19 comprising selectively updating a pixel of said frame based on either image data corresponding to the pixel being updated, or image data of a previously updated pixel.

25. The method of claim 24, wherein selectively updating said pixel comprises updating said pixel based on the image data of said previously updated pixel during said memory update time period.

26. The method of any one of claims 18-25, wherein correlating between said idle time period and said memory update time period comprises correlating between said idle time period and said memory update time period based on at least one timing signal corresponding to said frame.

27. The method of claim 26, wherein said at least one timing signal comprises at least one timing signal selected from the group consisting of a horizontal synchronization timing signal, a vertical synchronization timing signal, and a data enable timing signal.

28. The method of any one of claims 18-27, wherein said memory comprises a random access memory.

29. The method of any one of claims 18-28, wherein said memory comprises a look up table.

30. The method of any one of claims 18-29, wherein said memory comprises a single port memory.

31. The method of any one of claims 18-30, wherein said color image frame comprises a more-than-three primary color image frame.

32. The method of any one of claims 18-31, wherein the data stored in said memory comprises display parameter data.

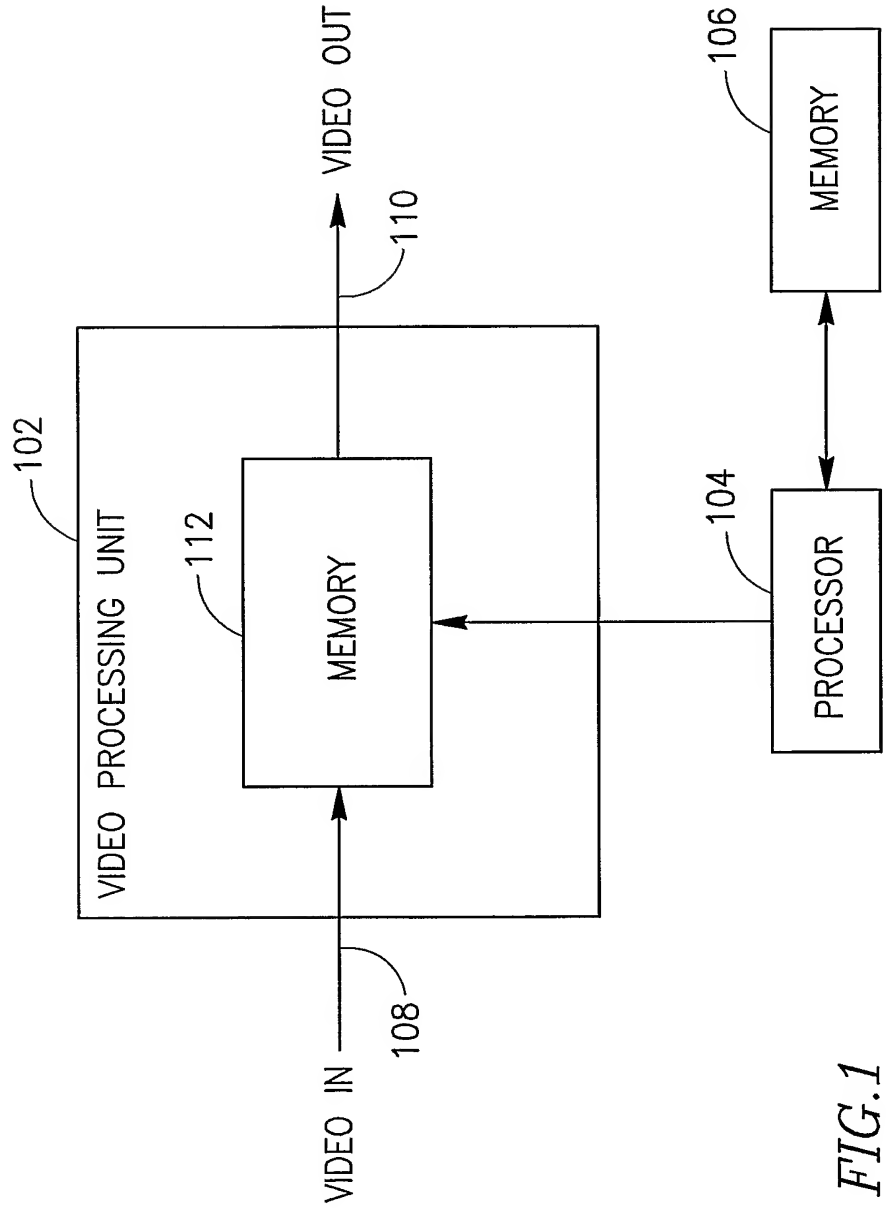

VIDEO OUT
110
106
MEMORY
102
VIDEO PROCESSING UNIT
112
MEMORY
104
PROCESSOR
VIDEO IN
108

FIG. 1

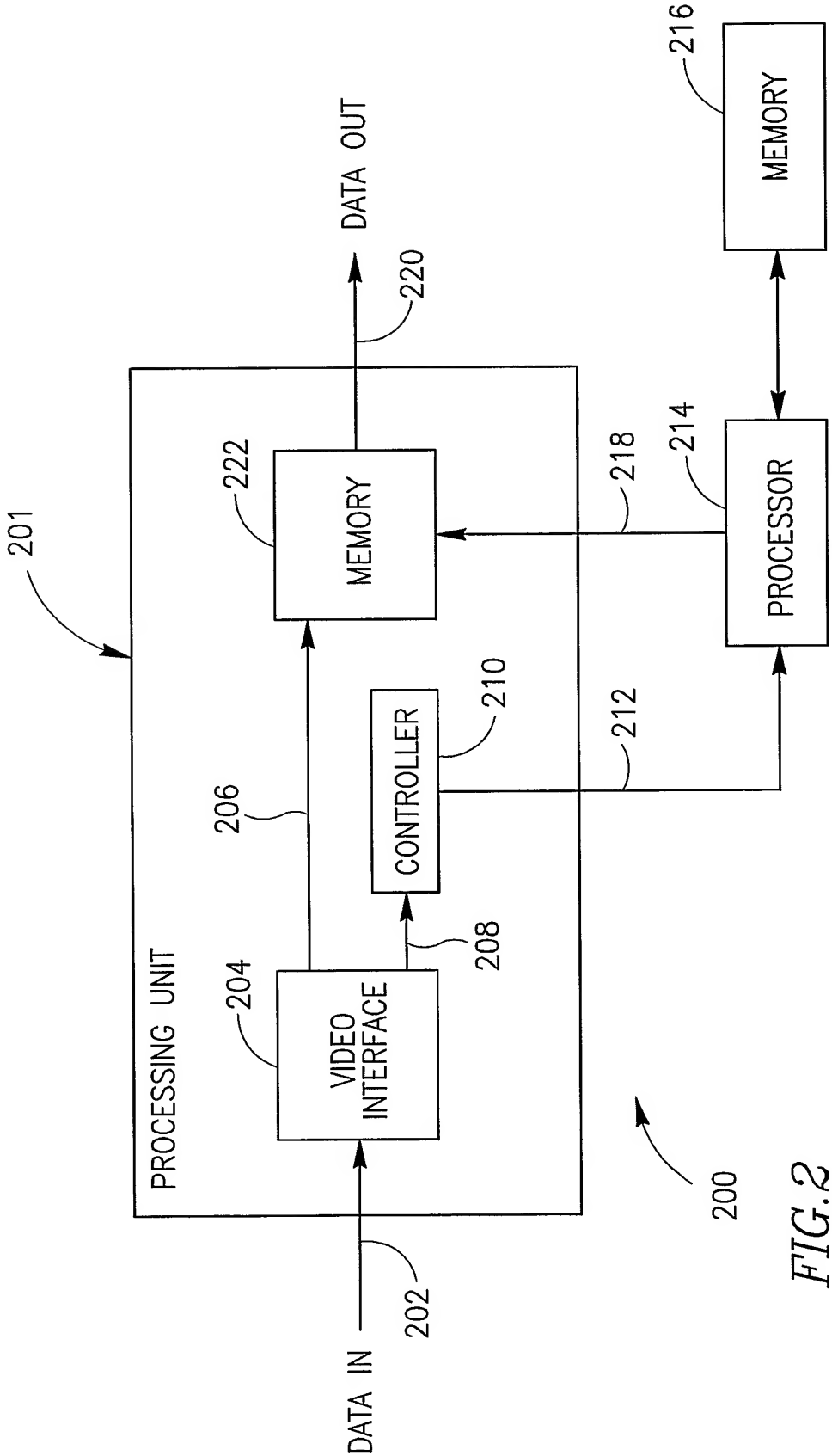
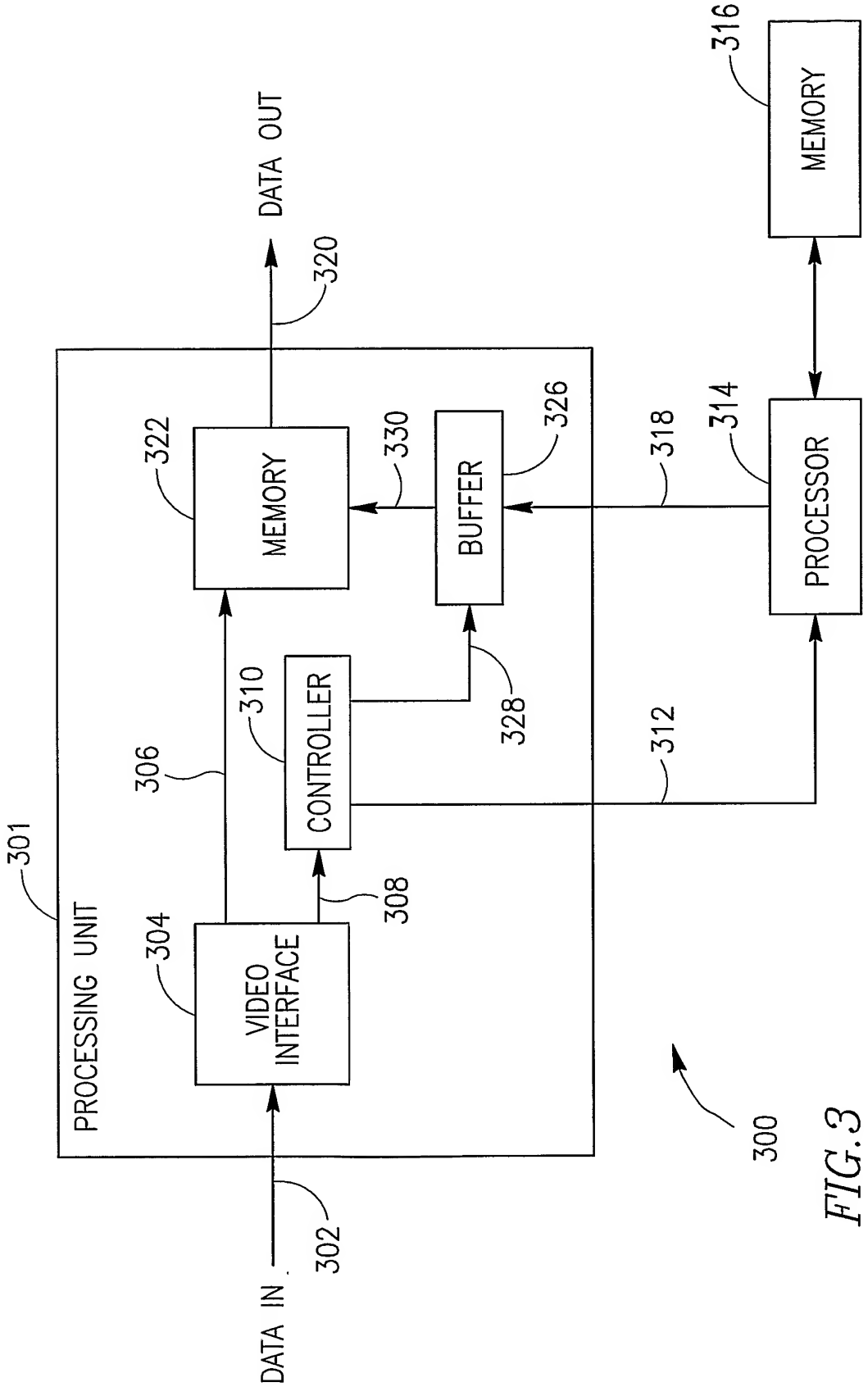

DATA IN
202
DATA OUT
220
PROCESSING UNIT
201
VIDEO INTERFACE
204
CONTROLLER
210
MEMORY
222
206
208
212
218
PROCESSOR
214
MEMORY
216
200

FIG.2


DATA IN
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DATA OUT
320
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301
VIDEO INTERFACE
304
CONTROLLER
310
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326
PROCESSOR
314
MEMORY
316
306
308
328
330
312
318
300

FIG.3

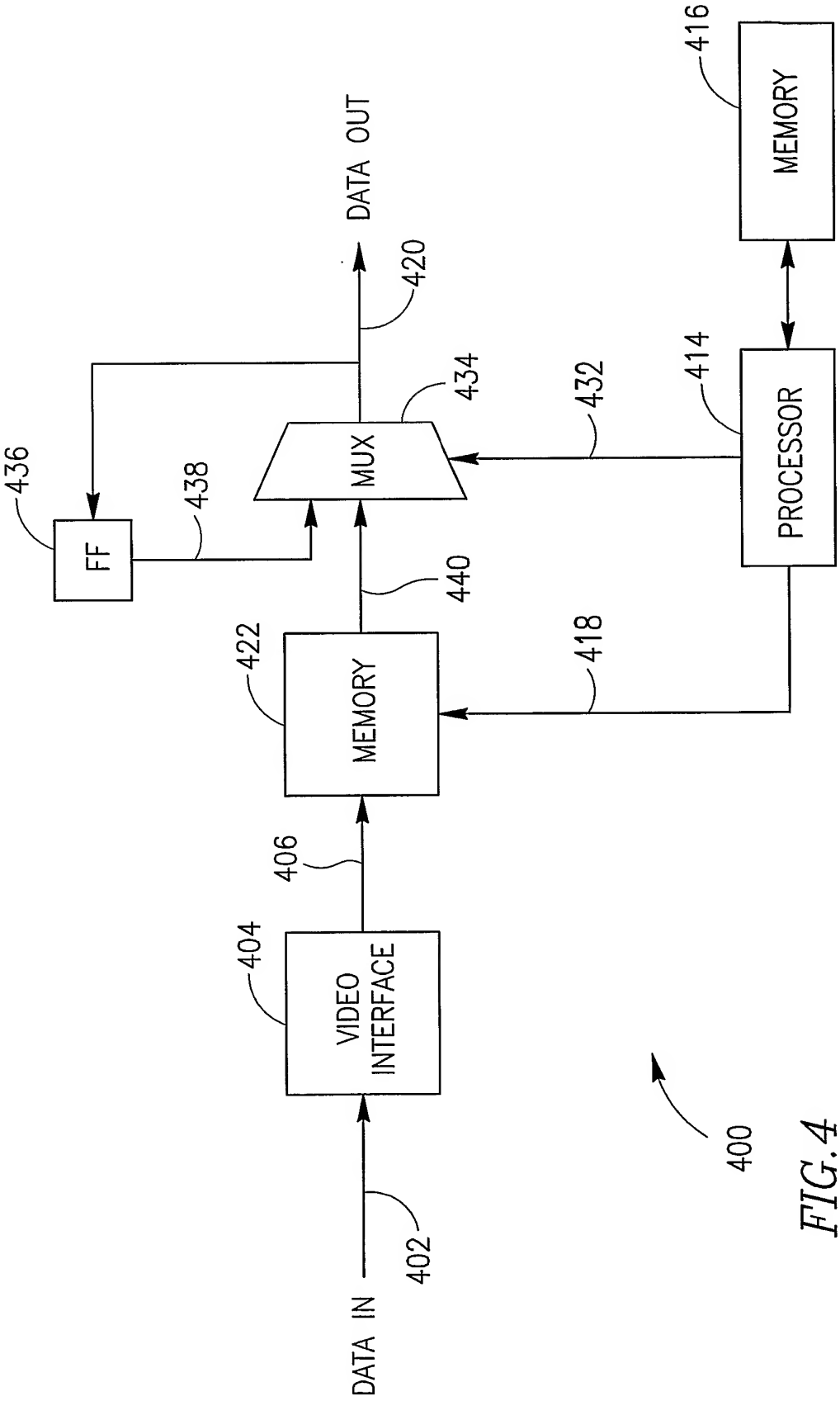
DATA IN
402
404
VIDEO INTERFACE
406
422
MEMORY
440
436
FF
438
MUX
434
DATA OUT
420
432
414
PROCESSOR
416
MEMORY
418
400

FIG. 4

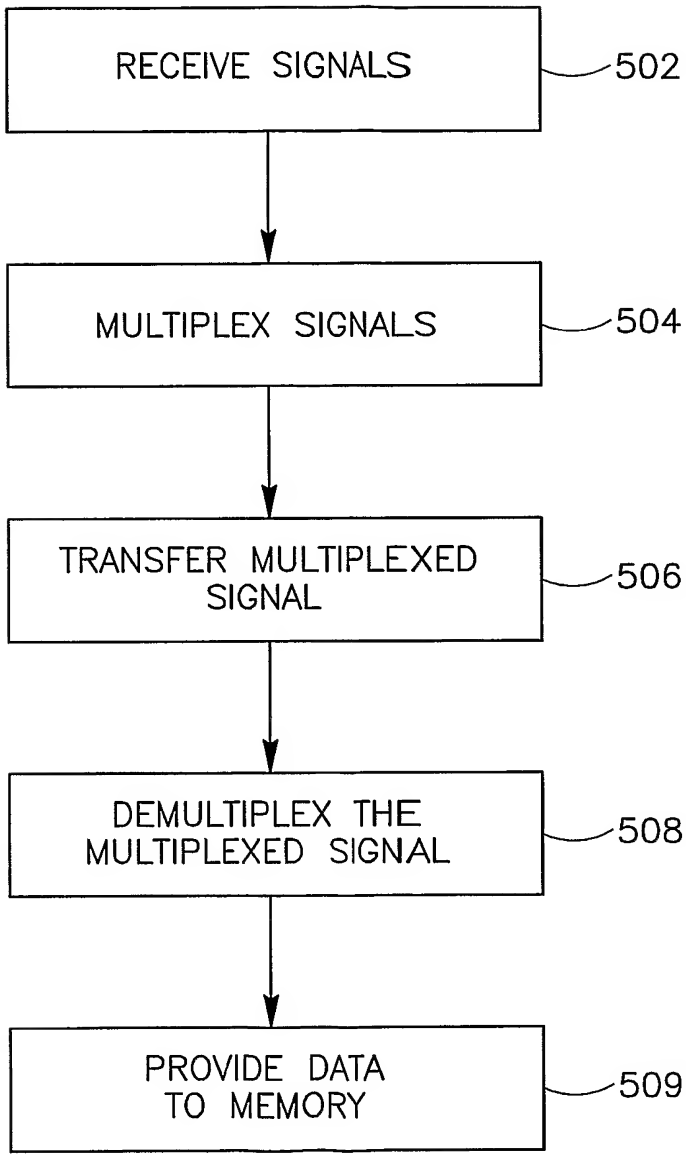
RECEIVE SIGNALS
502
MULTIPLEX SIGNALS
504
TRANSFER MULTIPLEXED SIGNAL
506
DEMULTIPLEX THE MULTIPLEXED SIGNAL
508
PROVIDE DATA TO MEMORY
509

FIG. 5

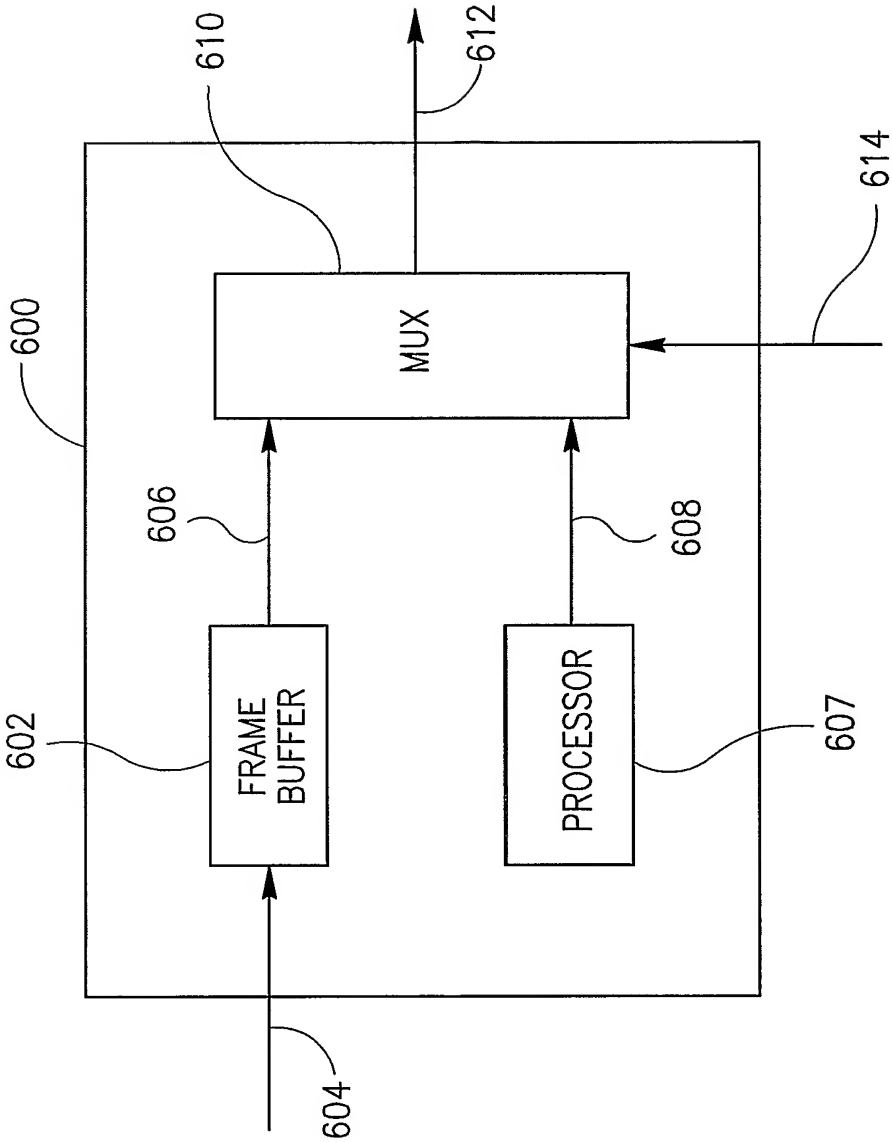
610
612
614
600
MUX
606
608
602
FRAME BUFFER
PROCESSOR
607
604

FIG.6

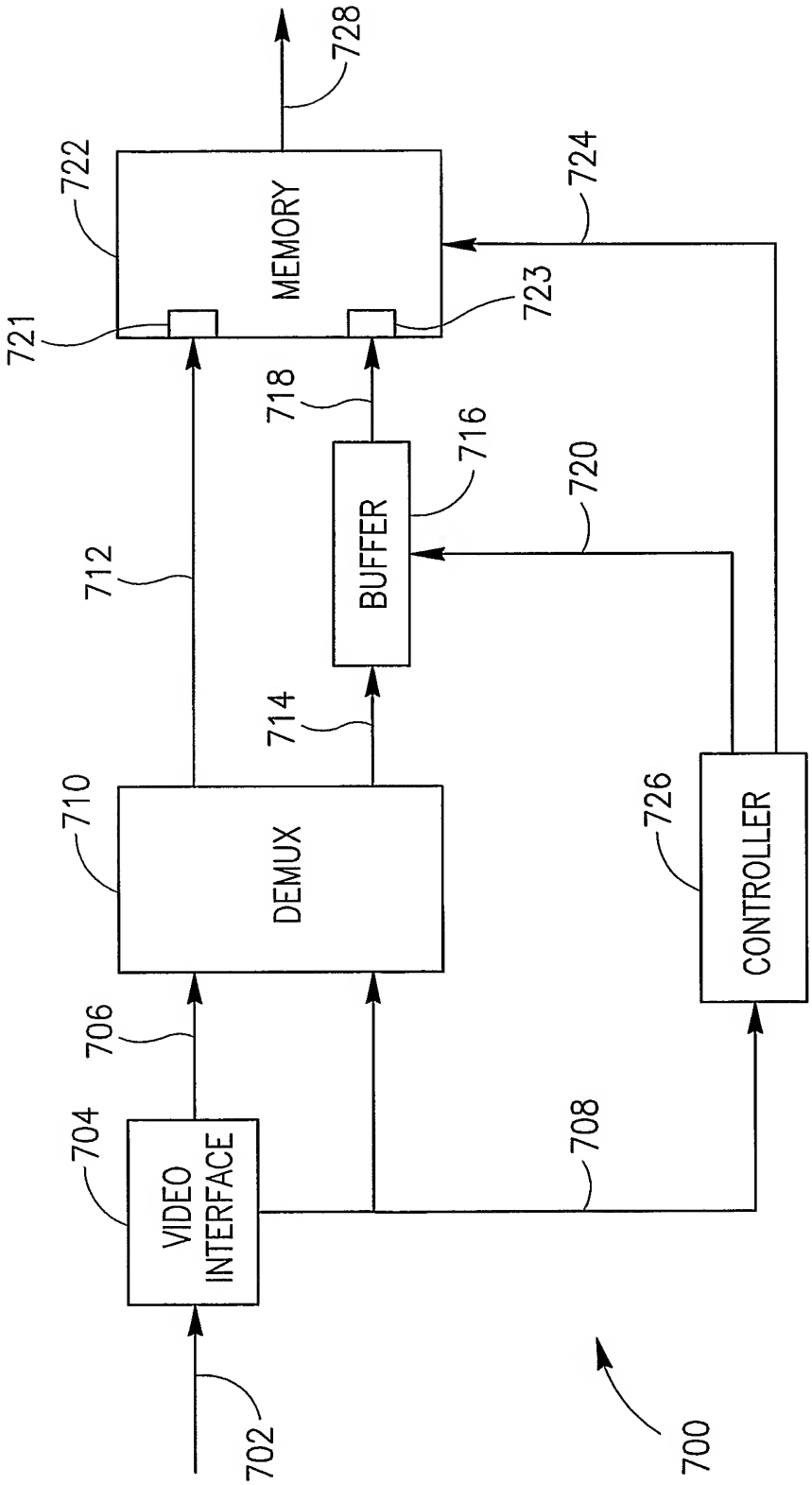
728
722
MEMORY
724
723
721
718
716
BUFFER
720
712
714
710
DEMUX
726
CONTROLLER
706
704
VIDEO INTERFACE
708
702
700

FIG. 7